REMARKS

Claims 1-2 are pending. By this Amendment, claims 3-4 are cancelled and claims 1-2 are amended.

The Office action rejects claims 1-4 under 35 U.S.C. § 102 over Ball (U.S. Pat. 5,583,855), rejects claims 1-4 under 35 U.S.C. § 102 over Furuta (U.S. Pat. 5,600,648), rejects claims 1-4 under 35 U.S.C. § 102 over Hurlocker (U.S. Pat. 5,490,142), rejects claims 1-4 under 35 U.S.C. § 102 over Yamamoto (U.S. Pat. 5,546,403), rejects claims 1-4 under 35 U.S.C. § 102 over Shioda (U.S. Pat. 5,537,393), rejects claims 1-4 under 35 U.S.C. § 102 over Lee (U.S. Pat. 5,799,001), rejects claims 1-4 under 35 U.S.C. § 102 over Hiramoto (U.S. Pat. 5,471,476), and rejects claims 1-2 under 35 U.S.C. § 102 over Takastu (U.S. Pat. 5,311,501).

These rejections are traversed as they apply to claims 1 and 2 and are moot in regards to claims 3-4, which have been cancelled.

Claims 1-2 have been amended to recite that the plurality of high-speed interface circuit packs and a plurality of low-speed interface circuit packs are connected to each other through said connecting circuit pack in a use mode of requiring a time slot assignment function alone (claim 1) and in a use mode of requiring a time slot assignment function and a time slot interchange function, a plurality of high-speed interface circuit packs and a plurality of low-speed interface circuit packs are connected to each other through said add/drop multiplex circuit pack (claim 2). As explained in the previous Response, these features are not disclosed by the cited references. Applicants thus request withdrawal of all pending rejections and allowance of claims 1 and 2.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made."**

The Office is authorized to charge any fees due under 37 C.F. R. § 1.17 or 1.18 to Deposit Account No. 11-0600.

Should there be any questions concerning this matter, the Examiner is invited to contact Applicants' undersigned attorney.

Respectfully submitted,

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APPENDIX

Version with Markings to Show Changes Made

IN THE CLAIMS:

Please cancel claims 3-4 without prejudice or disclaimer.

Please amend claims 1-2 as follows:

1. (Currently amended) A multiplex conversion unit comprising four types of circuit packs including a high-speed interface circuit pack, a low-speed interface circuit pack, an add/drop multiplex circuit pack and a connecting circuit pack, wherein:

said low-speed interface circuit pack accommodates one or a plurality of low-speed transmission lines and includes an output section for outputting a low-speed signal containing one or a plurality of time slots received from said low-speed transmission line to a plurality of high-speed interface circuit packs, and a path switch section for selecting one of the low-speed signals input from said high-speed interface circuit packs for each time slot as a low-speed signal to be transmitted to one or a plurality of said low-speed transmission lines accommodated;

said high-speed interface circuit pack accommodates at least a high-speed transmission line and is adapted to output/input a plurality of line signals each containing a predetermined number of time slots transmitted to and received from said high-speed transmission line accommodated, a plurality of line signals input/output by other high-speed interface circuit packs, and a plurality of low-speed signals input/output by said low-speed interface circuit packs, said high-speed interface circuit pack including a time slot assignment section having a first time slot assignment function between a plurality of line signals received from the said high-speed transmission line accommodated and output to other high-speed interface circuit packs on the one hand and the output low-speed signal on the other hand, and a second time slot assignment function between a plurality of line signals input from other high-speed interface circuit packs and

transmitted to the high-speed transmission line accommodated on the one hand and the input low-speed signal on the other hand;

said add/drop multiplex circuit pack is adapted to ~~out/input~~ output/input a plurality of line signals input/output by each of said high-speed interface circuit packs and a low speed signal containing one or a plurality of time slots input/output by each of the low-speed interface circuit packs, said add/drop multiplex circuit pack including a time slot section having the time slot interchange function between a plurality of line signals and a plurality of low-speed signals, and a line switch section having a first line switch function for switching the line signal to be processed by said time slot interchange section and a second lien switch function for switching the time slots of the line signal to be processed by said time slot interchange section using the time slot interchange function of said time slot interchange section;

said connecting circuit pack is adapted to input/output the low-speed signal input/output by the high-speed interface circuit pack as a low-speed signal input/output by another high-speed interface circuit pack; and

in a use mode of requiring a time slot assignment function alone, a plurality of high-speed interface circuit packs and a plurality of low-speed interface circuit packs are connected to each other through said connecting circuit pack in such a manner that the low-speed signals input/output by the high-speed interface circuit packs are input/output as low-speed signals input/output by another high-speed interface circuit pack.

2. (Currently amended) A multiplex conversion unit comprising four types of circuit packs including a high-speed interface circuit pack, a low-speed interface circuit pack, an add/drop multiplex circuit pack and a connecting circuit pack, wherein:

said low-speed interface circuit pack accommodates one or a plurality of low-speed transmission lines and includes an output section for outputting a low-speed signal containing one or a plurality of time slots received from said low-speed transmission line to a plurality of high-speed interface circuit packs, and a path switch section for selecting one of the low-speed signals input from said high-speed interface circuit packs for each

time slot as a low-speed interface circuit packs for each time slot as a low-speed signal to be transmitted to one or a plurality of said low-speed transmission lines accommodated;

said high-speed interface circuit pack accommodates at least a high-speed transmission line and is adapted to output/input a plurality of line signals each containing a predetermined number of time slots transmitted to and received from said high-speed transmission line accommodated, a plurality of line signals input/output by other high-speed interface circuit packs, and a plurality of low-speed signals input/output by said low-speed interface circuit packs, said high-speed interface circuit pack including a time slot assignment section having a first time slot assignment function between a plurality of line signals received from the said high-speed interface circuit packs on the one hand and the output low-speed signal on the other hand, and a second time slot assignment function between a plurality of line signals input from other high-speed interface circuit packs and transmitted to the high-speed transmission line accommodated on the one hand and the input low-speed signal on the other hand;

said add/drop multiplex circuit pack is adapted to output/input a plurality of line signals input/output by each of said high-speed interface circuit packs and a low-speed signal containing one or a plurality of time slots input/output by each of the low-speed interface circuit packs, said add/drop multiplex circuit pack including a time slot section having the time slot interchange function between a plurality of line signals and a plurality of low-speed signals, and a line switch section having a first line switch function for switching the line signal to be processed by said time slot interchange section and a second line switch function for switching the time slots of the line signal to be processed by said time slot interchange section using the time slot interchange function of said time slot interchange section;

said connecting circuit pack is adapted to input/output the low-speed signal input/output by the high-speed interface circuit pack as a low-speed signal input/output by another high-speed interface circuit pack; and

in a use mode of requiring a time slot assignment function and a time slot interchange function, a plurality of high-speed interface circuit packs and a plurality of

low-speed interface circuit packs are connected to each other through said add/drop multiplex circuit pack, and

the time slot assignment section of said high-speed interface circuit packs has the add/drop multiplex function of converting the line signals transmitted to and received from the high-speed transmission line into a plurality of low-speed signals directly output/input, ~~the connecting circuit pack in the first mode is replaced by an add/drop multiplex circuit pack,~~ and the high-speed interface pack and the low-speed interface circuit pack are connected to the add/drop multiplex circuit pack in such a manner that a plurality of low-speed signals input/output by a plurality of high-speed interface circuit packs are output/input by said add/drop multiplex circuit pack as line signals output/input by a plurality of high-speed interface circuit packs, and the low-speed signals input/output by the add/drop multiplex circuit pack are output/input by the low-speed interface circuit pack as output/input low-speed signals.